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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,787	01/30/2004	Colin Murgatroyd	920476-95496	7138

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EXAMINER	
ELALLAM, AHMED	

ART UNIT	PAPER NUMBER
2616	

NOTIFICATION DATE	DELIVERY MODE
07/08/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patent-ch@btlaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/768,787	MURGATROYD ET AL.	
	Examiner	Art Unit	
	AHMED ELALLAM	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-23 and 25-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,13,15-23,25-30 and 34-40* is/are rejected.

7)☐ Claim(s) *10-12, 14, 31-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is responsive to Amendment filed on 03/13/2008. The Amendment has been entered. Claims 1, 2, 4-23, 25-40 are pending.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-2, 4-6, 8, 20-23, 25-27, 29, and 36-40 are rejected under 35 U.S.C. 102(e) as being anticipated by Iryami et al, US 7,032,139 B1. Hereinafter referred to as Iryami.

Regarding claims 1, 20, 36 with reference to figures 2, 4B and 4C, Iryami discloses a method/ a bit error tester 100 (Figure 2) and a control logic 225 (Figure 2) for performance monitoring in a communications network, comprising:

Measuring bit error rate of a signal over time by allocating bit error thresholds selected from a plurality of bit error rate thresholds, the thresholds corresponding to triggering events, see figure 4B and 4C, column 9, lines 63-column 10, line 29. (claimed monitor or monitoring a signal over time by allocating a current signal quality characterization to the signal, selected from at least two such signal quality characterizations; identifying a plurality of time intervals making up a continuous succession of such time intervals, such that a current time interval is terminated and a next time interval is initiated each time the signal quality characterization allocated to

the signal changes). Iryami further discloses generating a log that describe each triggering event and data relating to these triggering events is captured and stored, see column 10, lines 13-15, and lines 27-29. (Claimed generating a record of each identified time interval).

Irami, with reference to figure 4C, it is shown a period of time during which the bit error rate is null. (Claimed signal quality characterization comprise a perfect time interval). Irami also discloses triggering event (used for data capture for analysis) may be the bit error rate crossing a particular threshold (e.g., 10.sup.-12 errors/second or 10.sup.-9 errors/second). See column 7, lines 66-column 8, and line 6. (Corresponding to the claimed selected two signal quality characterizations).

Regarding claims 2, 23, Iryami discloses generating a log that describe each triggering event and data relating to these triggering events is captured and stored, see column 10, lines 13-15. (Claimed generating a performance log using the records).

Regarding claims 4, and 25 , Iryami discloses generating a log that describe each triggering event and data relating to these triggering events is captured and stored, see column 10, lines 13-15.

Regarding claims 5 and 26, figure 4C shows a time axis including intervals of time and corresponding bit error time. (Claimed record for each interval comprises at least the length of the interval and the signal quality characterization allocated for the interval).

Regarding claims 6 and 27, Iryami discloses generating a log that describe each triggering event, so that a user can analyze each event. See column 10, lines 13-15.

(Claimed generating a performance log made up of records stored in accordance with the succession of time intervals).

Regarding claims 8 and 29, Figure 4C of Iryami provides for sets of records corresponding to continuous successions of time intervals. (Claimed sets of records corresponding to continuous successions of time intervals).

Regarding claims 21 and 22, Iryami discloses a processor belonging to the bit error tester 100, Figure 2, unit 225. The bit error tester 100 have multiple network interfaces to which different types of networks may connect. See column 1, lines 56-58. (Claimed processor is located in a network element of the communications network, as in claim 21, and processor for monitoring a communications path and which is located in a network element of the communications network, which network element terminates the communications path).

Regarding claims 37 and 40, Iryami discloses the control logic in the bit error tester, see figure See figure 2. (Claimed control logic is located in a network element of the communications network).

Regarding claim 38, Iryami discloses monitoring a communications path and which is located in a network element of the communications network, which network element terminates the communications path. See Figure 1.

Regarding claim 39, Iryami discloses the bit error tester (claimed network element) for carrying out performance monitoring in a communications network comprising; control logic 225, memory 215 and comparator 220, these element in

cooperation provides the means for implementing the method of Iryami as discussed in claim 1 above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iryami.

Regarding claims 17, 18 and 19:

Claim 17 is a computer executable software code stored on a computer readable medium for making a computer execute the method of claim 1.

Claim 18 is a programmed computer, which stores computer executable program code for making the computer execute the method of claim 1.

Claim 19 is computer readable medium having computer executable software code stored thereon, which code is for making a computer execute the method of claim 1.

Examiner take official notice that executing a method using a computer executable software code stored on a computer readable medium (as in claim 17), or a programmed computer, which stores computer executable program code for making the

computer implement a method steps (as in claim 18), or computer readable medium having computer executable software code stored thereon, which code is for making a computer execute a method steps, as in claim 19, are well known in the art. Since official action is taken, it would have been obvious to a person of skill in the art at the time the invention was made to implement his method using computer media so that the method can be implemented using software so to reduce the cost and time required for a hardware implementation.

3. Claims 7, 9, 13, 15 and 16, 28, 30, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iryami in view of McGee et al, US 2003/0088542. Hereinafter referred to as McGee.

Regarding claims 7, 9, 13, 15 and 16, 28, 30, 34 and 35 Iryami Does not disclose manipulating selected records to reduce the amount of memory required to store the records while intelligently degrading their accuracy, as in claim 7 and 28, designating some records as primary records and others as secondary records; selecting sets of secondary records corresponding to continuous successions of time intervals; and merging the selected sets to form a merged record as in claims 9 and 30, and monitoring the amount of memory required to store the records, and when the amount of memory reaches a predetermined limit, selecting sets of records corresponding to continuous successions of time intervals, and merging the selected sets to form a merged record so as to reduce the amount of memory required to store the records as in claims 13 and 34, and merging selected records to form a merged record with a quality characterization of poor time and a duration equal to the sum of the duration of

the intervals associated with the merged records, as in claims 15 and 35, and selecting a set of records corresponding to a continuous succession of time intervals and merging the selected set to form a merged record provided the memory required to store the merged record is less than the memory required to store the selected set of records as in claim 16.

However, McGee discloses in the same field of endeavor of approximating monitored values for a network performance data storage, (paragraph [0082]), merging plurality of data sets with reduced data storage requirements. See paragraph [0016].

It would have been obvious to a person of skill in the art at the time the invention was made to merge the data records of Iryami in accordance with the merging method of McGee so to reduce storage capacity (McGee [0082]). It would be also advantageous to greatly reduce the number of calculations that are needed to produce useful records for the network performance data (histograms). (McGee [0082]).

Allowable Subject Matter

4. Claims 10-12, 14, 31-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed 03/13/2008 have been fully considered but they are not persuasive:

Applicants argue that "*Iryami fails to disclose the generation of a record of time intervals, in which a time interval is defined as a period of time during which an error level, particularly one of the specific error characterizations now specified in the independent claims, remains constant. Thus, Iryami fails to disclose the time interval records as now claimed, and which can enable a low data volume log to be generated*". Emphasis added.

Examiner respectfully disagrees, Iryami discloses

Measuring bit error rate of a signal over time by allocating bit error thresholds selected from a plurality of bit error rate thresholds, the thresholds corresponding to triggering events, see figure 4B and 4C, column 9, lines 63-column 10, line 29. Iryami also discloses generating a log that describe each triggering event and data relating to these triggering events is captured and stored, see column 10, lines 13-15, and lines 27-29. Iryami, Further shows with reference to figure 4C, a period of time during which the bit error rate is null (corresponding to claimed signal quality characterization comprise a perfect time interval). Iryami also discloses triggering event (used for data capture for analysis) may be the bit error rate crossing a particular threshold (e.g., 10.sup.-12 errors/second or 10.sup.-9 errors/second). See column 7, lines 66-column 8, and line 6. (Corresponding to the claimed selected two signal quality characterizations). It should be noted that Iryami associate the triggering events' thresholds with the bit error rate values (e.g., 10.sup.-12 errors/second or 10.sup.-9 errors/second), the values (error rates) associated with the threshold correspond to the claimed "**signal quality characterizations**". The difference between Iryami and Applicants is a matter of

lexicography. Iryami did not choose to specify at least two thresholds associated triggers with his own terms such as Perfect Time Interval, and Errored Time Interval. Iryami, however as discussed above, discloses signals with null time intervals, and signal with measured the bit error rate of 10.sup.-12 errors/second which can be considered as an Errored Time Interval.

Examiner asserts that Iryami anticipates the invention as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AHMED ELALLAM whose telephone number is (571)272-3097. The examiner can normally be reached on 7-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on (571) 272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/AHMED ELALLAM/
Examiner, Art Unit 2616
6/30/08

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7/2/08